IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
DUBORGEL

Serial No. **NOT YET ASSIGNED**

Filing Date: **HEREWITH**

For: **MICROARCHITECTURE OF AN ARITHMETIC UNIT**

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASST. COMMISIONER FOR PATENTS, WASHINGTON DC 20231-0001.

EXPRESS MAIL NO: EL 768537499 US

DATE OF DEPOSIT: December 28, 2001

NAME: DAWN KIMLER

SIGNATURE: Dawn Kimler

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to label FIG. 1 as prior art.

In the Claims:

Please cancel Claims 1 to 10.

Please add new Claims 11 to 37.

11. A microarchitecture for an arithmetic unit, said arithmetic unit being defined to generate a result of N bits ranked 0 to N-1 of an addition of at least two input operands,

and one corresponding output carry bit, said microarchitecture comprising:

an N+1 bit accumulator;

an N+1 bit carry save adder for providing two output vectors from the at least two input operands, one of the operands corresponding to a current contents of the accumulator;

an N+1 bit final adder receiving the output vectors at input and generating a corresponding result at output; and

a determining circuit for receiving a most significant bit of the result generated by said final adder and a most significant bit of the operand corresponding to the current contents of the accumulator and determining the output carry bit.

12. A microarchitecture of an arithmetic unit according to Claim 11, wherein said carry save adder receives a first operand, a second operand and a third operand as inputs, the third operand corresponding to the current contents of the accumulator; and wherein said determining circuit comprises an evaluation circuit for evaluating a most significant bit of a sum of the first and second input operands.

13. A microarchitecture according to Claim 12, wherein said evaluation circuit comprises an adder for generating the most significant bit of the sum of the first and second input operands.

14. A microarchitecture according to Claim 12, wherein the determining circuit comprises a logic circuit that outputs the output carry value based upon the most significant bit of the sum of the first and second input operands generated by said evaluation circuit, the N-ranked bit of the current contents of the accumulator and the N-ranked bit of the result generated by the final adder.

15. A microarchitecture according to Claim 12, further comprising a multiplier for generating partial products of two operands applied as inputs to the arithmetic unit, wherein the partial products are applied as the first and second input operands of the carry save adder.

16. A microarchitecture according to Claim 12, further comprising a concatenation circuit for the concatenation of two operands input to the arithmetic unit, and generating a concatenated number at output, to carry out operations of double precision accumulation with the current contents of the accumulator, the concatenated number being applied as the first input operand of said carry save adder, said second input operand being set at the zero vector.

17. A microarchitecture according to Claim 15, further comprising:

a concatenation circuit, connected in parallel with the multiplier, for the concatenation of two operands input to the arithmetic unit, and generating a concatenated number at

output, to carry out operations of double precision accumulation with the current contents of the accumulator; and

a multiplexer connected to the multiplier and the concatenation circuit for selectively applying either the concatenated number and a zero vector or the partial products as the first and second input operands of the carry save adder.

18. A microarchitecture according to Claim 17, wherein the determining circuit comprises a second multiplexer for selectively providing, as an evaluated bit, either the bit generated by the evaluation circuit or the most significant bit of the concatenated number.

19. A microarchitecture according to Claim 12, further comprising a format extension circuit for extending the operands applied as first and second input operands of the carry save adder to N^{+1} bits, wherein the evaluation circuit receives the first and second input operands before format extension.

20. A microprocessor comprising:

an arithmetic unit for generating a result of N bits of an addition of at least two input operands, and one corresponding output carry bit, said arithmetic unit comprising

an N+1 bit accumulator;

an N+1 bit carry save adder for providing two output vectors from the at least two input operands,

one of said operands corresponding to a current contents of the accumulator;

an N+1 bit final adder receiving the output vectors at input and generating a corresponding result at output; and

a determining circuit for receiving a most significant bit of the result generated by said final adder and a most significant bit of the operand corresponding to the current contents of the accumulator and determining the output carry bit.

21. A microprocessor according to Claim 20, wherein said carry save adder receives a first operand, a second operand and a third operand as inputs, the third operand corresponding to the current contents of the accumulator; and wherein said determining circuit comprises an evaluation circuit for evaluating a most significant bit of a sum of the first and second input operands.

22. A microprocessor according to Claim 21, wherein said evaluation circuit comprises an adder for generating the most significant bit of the sum of the first and second input operands.

23. A microprocessor according to Claim 21, wherein the determining circuit comprises an exclusive-or type logic circuit that outputs the output carry value based upon the most significant bit of the sum of the first and second input operands generated by said evaluation circuit, an N-ranked bit

of the current contents of the accumulator and an N-ranked bit of the result generated by the final adder.

24. A microprocessor according to Claim 21, further comprising a multiplier for generating partial products of two operands applied as inputs to the arithmetic unit, wherein the partial products are applied as the first and second input operands of the carry save adder.

25. A microprocessor according to Claim 21, further comprising a concatenation circuit for the concatenation of two operands input to the arithmetic unit, and generating a concatenated number at output, to carry out operations of double precision accumulation with the current contents of the accumulator, the concatenated number being applied as the first input operand of said carry save adder, said second input operand being set at the zero vector.

26. A microprocessor according to Claim 24, further comprising:

a concatenation circuit, connected in parallel with the multiplier, for the concatenation of two operands input to the arithmetic unit, and generating a concatenated number at output; and

a multiplexer connected to the multiplier and the concatenation circuit for selectively applying either the concatenated number and a zero vector or the partial products as the first and second input operands of the carry save adder.

27. A microprocessor according to Claim 26, wherein the determining circuit comprises a second multiplexer for selectively providing, as an evaluated bit, either the bit generated by the evaluation circuit or the most significant bit of the concatenated number.

28. A microprocessor according to Claim 21, further comprising a format extension circuit for extending the operands applied as first and second input operands of the carry save adder to N^{+1} bits, wherein the evaluation circuit receives the first and second input operands before format extension.

29. A method of generating a result of N bits of an addition of at least two input operands, and one corresponding output carry bit with an arithmetic unit, the method comprising:

providing an N+1 bit accumulator;

providing two output vectors from the at least two input operands with an N+1 bit carry save adder, one of the operands corresponding to a current contents of the accumulator;

generating the result at an output of an N+1 bit final adder which receives the output vectors at input; and

determining the output carry bit with a determining circuit which receives a most significant bit of the result generated by the final adder and a most significant bit of the

operand corresponding to the current contents of the accumulator.

30. A method according to Claim 29, wherein said carry save adder receives a first operand, a second operand and a third operand as inputs, the third operand corresponding to the current contents of the accumulator; and wherein said determining circuit comprises an evaluation circuit for evaluating a most significant bit of a sum of the first and second input operands.

31. A method according to Claim 30, wherein said evaluation circuit comprises an adder for generating the most significant bit of the sum of the first and second input operands.

32. A method according to Claim 30, wherein the determining circuit comprises an exclusive-or type logic circuit that outputs the output carry value based upon the most significant bit of the sum of the first and second input operands generated by said evaluation circuit, the N-ranked bit of the current contents of the accumulator and the N-ranked bit of the result generated by the final adder.

33. A method according to Claim 30, further comprising generating partial products of two operands applied as inputs to the arithmetic unit with a multiplier, wherein the partial products are applied as the first and second input operands of the carry save adder.

34. A method according to Claim 30, further comprising concatenating two operands input to the arithmetic unit with a concatenation circuit to generate a concatenated number which is applied as the first input operand of said carry save adder, said second input operand being set at the zero vector.

35. A method according to Claim 33, further comprising:

concatenating two operands input to the arithmetic unit with a concatenation circuit connected in parallel with the multiplier, to generate a concatenated number; and

selectively applying either the concatenated number and a zero vector or the partial products as the first and second input operands of the carry save adder with a multiplexer connected to the multiplier and the concatenation circuit.

36. A method according to Claim 35, wherein the determining circuit comprises a second multiplexer for selectively providing, as an evaluated bit, either the bit generated by the evaluation circuit or the most significant bit of the concatenated number.

37. A method according to Claim 30, further comprising extending the operands applied as first and second input operands of the carry save adder to N^{+1} bits with a format extension circuit, wherein the evaluation circuit

receives the first and second input operands before format extension.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination, a Notice of Allowance is respectfully requested in due course. If any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

PAUL J. DITMYER
Reg. No. 40,455
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330
407-841-2343 fax
Attorneys for Applicants

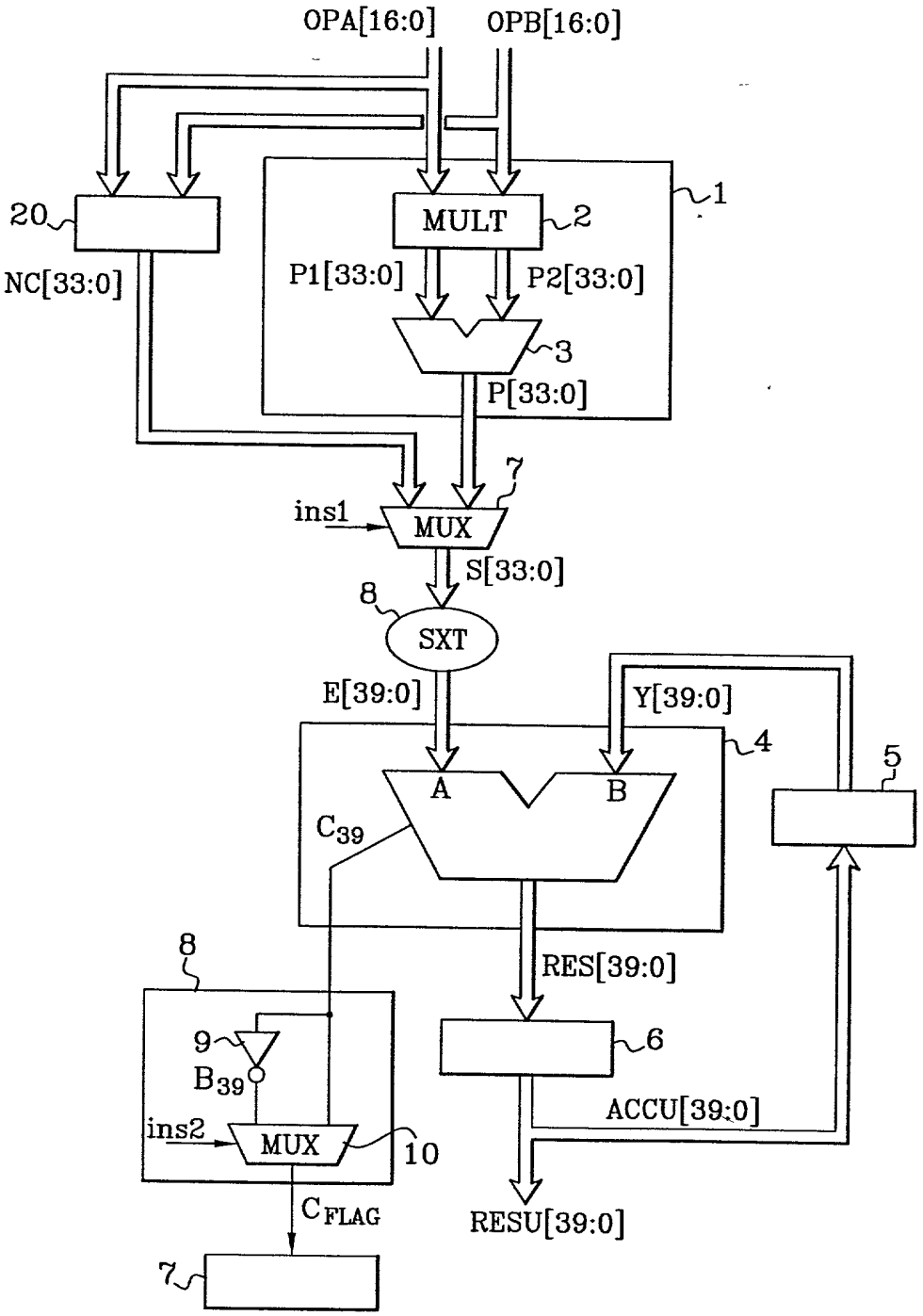

Fig. 1

PRIOR ART

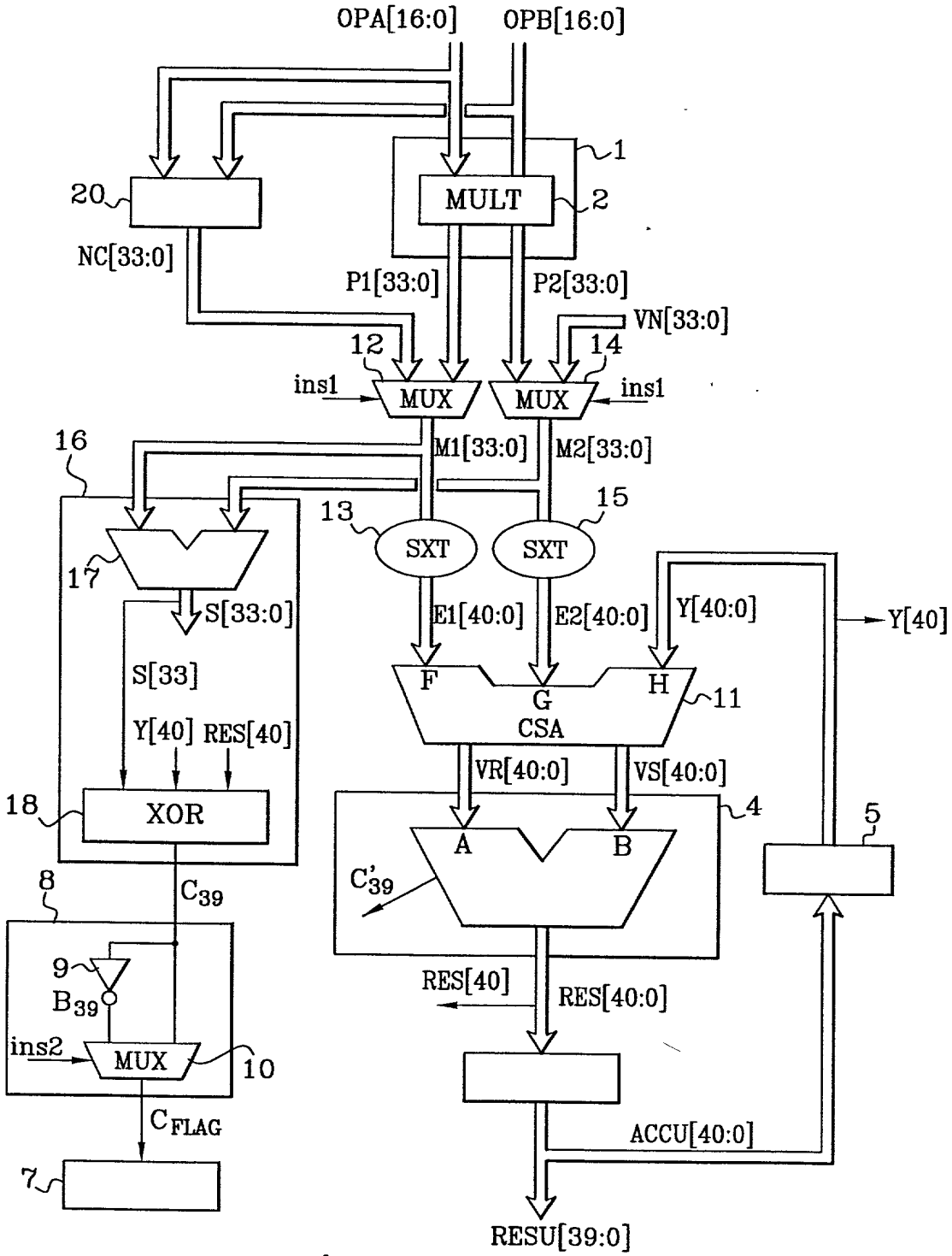
OPA[16:0]
OPB[16:0]
1
MULT
2
20
NC[33:0]
P1[33:0]
P2[33:0]
VN[33:0]
12
14
ins1
MUX
MUX
ins1
16
M1[33:0]
M2[33:0]
13
15
SXT
SXT
17
S[33:0]
E1[40:0]
E2[40:0]
Y[40:0]
Y[40]
S[33]
F
G
H
11
CSA
Y[40]
RES[40]
VR[40:0]
VS[40:0]
18
XOR
4
5
A
B
8
C39
C'39
9
B39
RES[40]
RES[40:0]
ins2
MUX
10
CFLAG
ACCU[40:0]
7
RESU[39:0]

Fig. 2

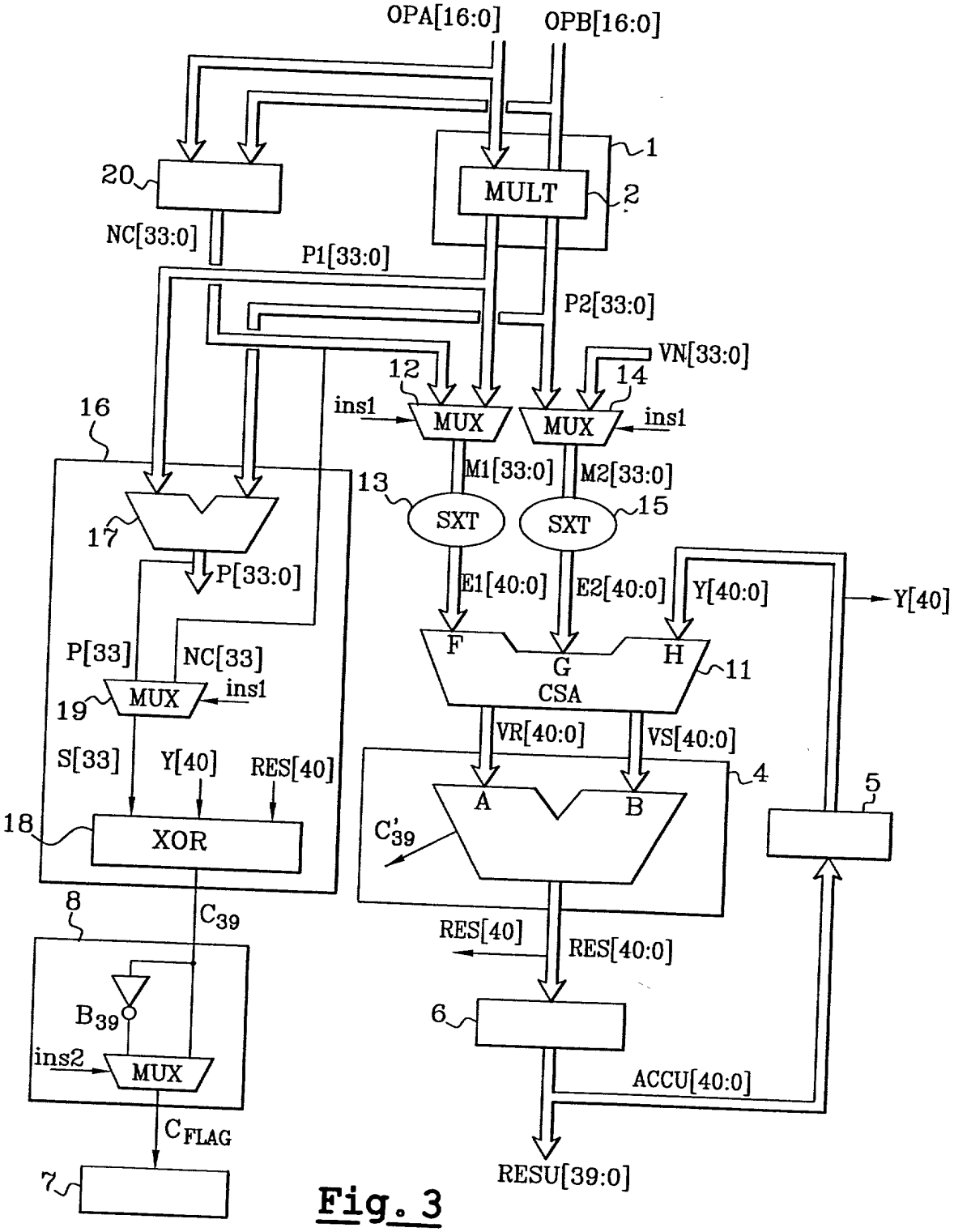
OPA[16:0]
OPB[16:0]
1
20
MULT
2
NC[33:0]
P1[33:0]
P2[33:0]
VN[33:0]
12
14
16
ins1
MUX
MUX
ins1
M1[33:0]
M2[33:0]
13
SXT
SXT
15
17
P[33:0]
E1[40:0]
E2[40:0]
Y[40:0]
Y[40]
F
G
H
11
CSA
P[33]
NC[33]
MUX
ins1
19
VR[40:0]
VS[40:0]
S[33]
Y[40]
RES[40]
4
5
A
B
18
XOR
C'39
8
C39
RES[40]
RES[40:0]
B39
6
ins2
MUX
ACCU[40:0]
CFLAG
7
RESU[39:0]

Fig. 3